

**CPU CORE**

VCC\_CORE

ISL6262A Page:25

**+3VPCU  
+3V\_S5/+3VSUS  
+3V  
+5VSUS/+5V  
10V/15V  
+1.8V\_S5**

+3VPCU  
+3V\_S5  
+3VSUS  
+3V  
+5VSUS  
+5V  
10V/15V  
+1.8V\_S5

MAXIM  
MAX8744ETJ+ Page:26

**+1.8VSUS/+1.8V  
+1.2V**

+1.8VSUS  
+1.8V  
+1.2V

MAXIM  
MAX8743EEI Page:27

**+1.05V**

+1.05V

SENTECH  
SC4215\*2 Page:29

**+0.9VSUS  
+0.9V**

+0.9VSUS  
+0.9V

GMT  
G2996 Page:26,29

**BATTERY CHARGER**

MAXIM  
MAX8724 Page:28

**Power State Table**

Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+5VPCU	N/A	ALWAYS	VIN
+5V_S5	S5_ON	S0-S5	+5VPCU
+5VSUS	SUSON	S0-S3	+5VPCU
+5V	MAINON	S0	+5VPCU
15V/10V	N/A	S0	+5VPCU
+1.2V	MAINON	S0	VIN
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS
+1.5V	MAINON	S0	+3V

**CLOCK GEN  
RTM865-300**

+3V Page:4

**PL5**

**Yonah /Merom**

INTEL Mobile\_479 CPU  
SOCKET\_M Page:2, 3

**DDR-II SODIMM1**

Page: 9

**DDR-II SODIMM2**

Page: 9

400M/533M/667M HZ

**NB  
RC410ME  
ATI**

Page: 5, 6, 7, 8

**SATA HDD**

Page: 18

**IDE-ODD**

Page: 18

**SB  
ATi SB450**

Page: 11, 12, 13, 14

**AUDIO CODEC  
REALTEK  
ALC861**

Page: 19

**GMT  
G1432+G1410**

Page: 20

**MODEM  
AGERE  
DELPHI-MOM**

Page: 21,22

**KBC  
NS  
PC97551**

Page: 23

**MIC IN**

Page: 20

**SPEAKER**

Page: 20

**LINE OUT**

Page: 20

**RJ11**

Page: 20

**Touchpad**

Page: 24

**Keyboard**

Page: 24

**FLASH**

Page: 24

**FAN**

Page: 24

**ENE PCMCIA  
CB1410 (option)**

AD17  
REQ3# / GNT3#  
INTE#  
Page: 16

**TYPE II  
SLOT**

Page: 16

**MINI-PCI  
Wireless LAN**

AD20  
REQ1# / GNT1#  
INTG# , INT#  
Page: 17

**REALTEK  
RTL8100CL**

AD18  
REQ0# / GNT0#  
INTF#  
Page: 15

**BOTHHAND  
TRANSFORMER  
NS0013**

Page: 15

**RJ45**

Page: 15

**SYSTEM  
USB PORT \*1**

Page: 17

**Connector**

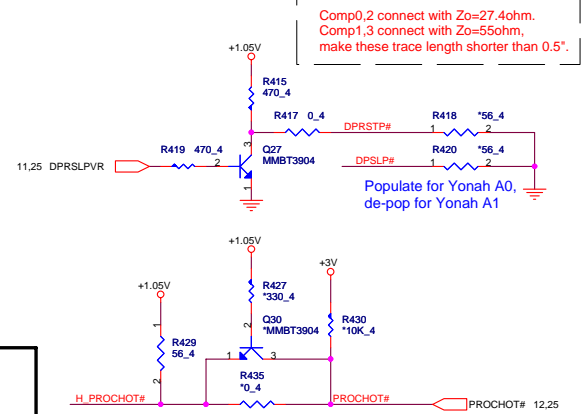
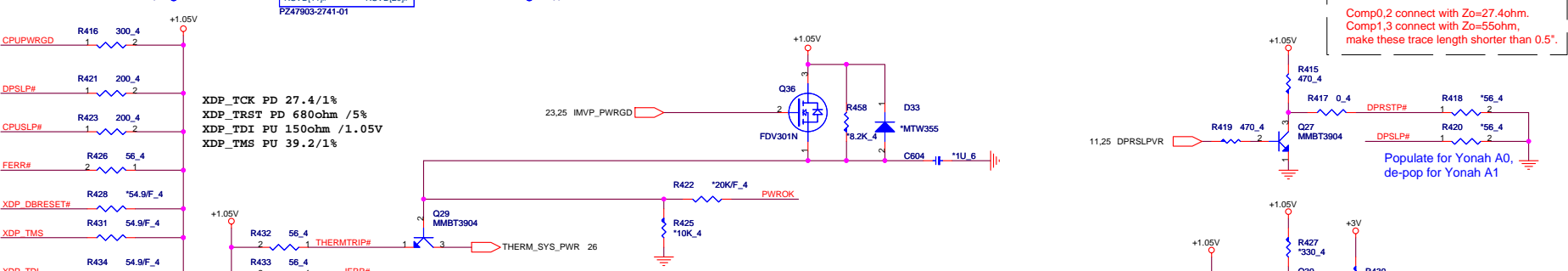
**USB BOARD  
USB PORT \*2**


Page: 17

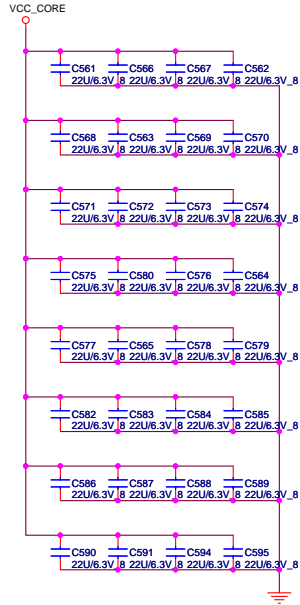
**PROJECT : PL5**

**Quanta Computer Inc.**

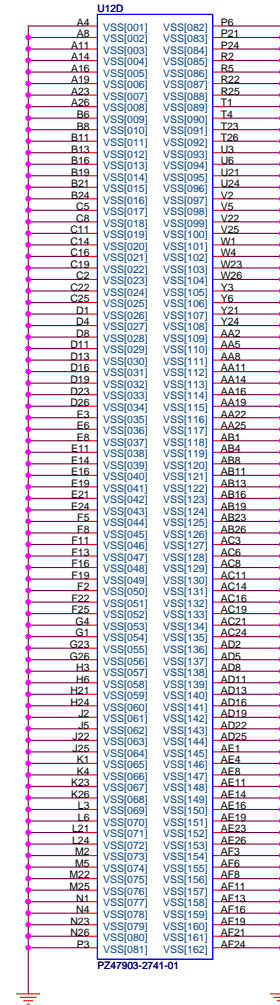
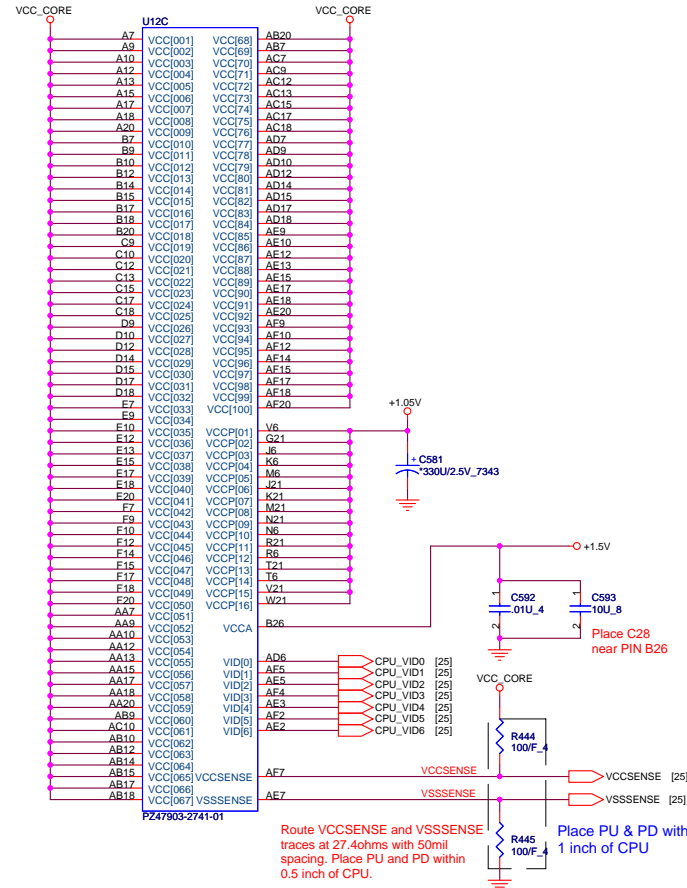
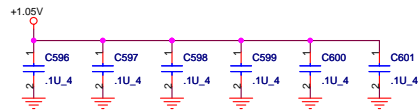
Size	Document Number	Rev
	<b>BLOCK DIAGRAM</b>	1A
Date:	Thursday, December 07, 2006	Sheet 1 of 30



 <div style="text-align: right;"> <b>PROJECT : PL5</b>  <b>Quanta Computer Inc.</b> </div>		
Size	Document Number <b>Yanah CPU(HOST Bus)-1</b>	Rev <b>1A</b>
Date:	Saturday, December 23, 2006	Sheet 2 of 30

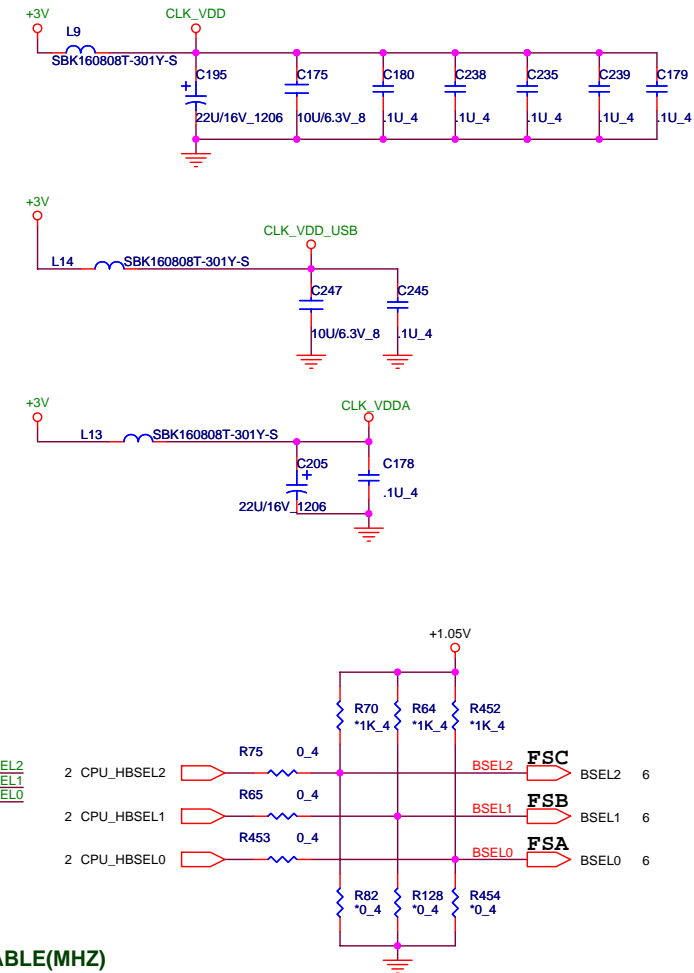
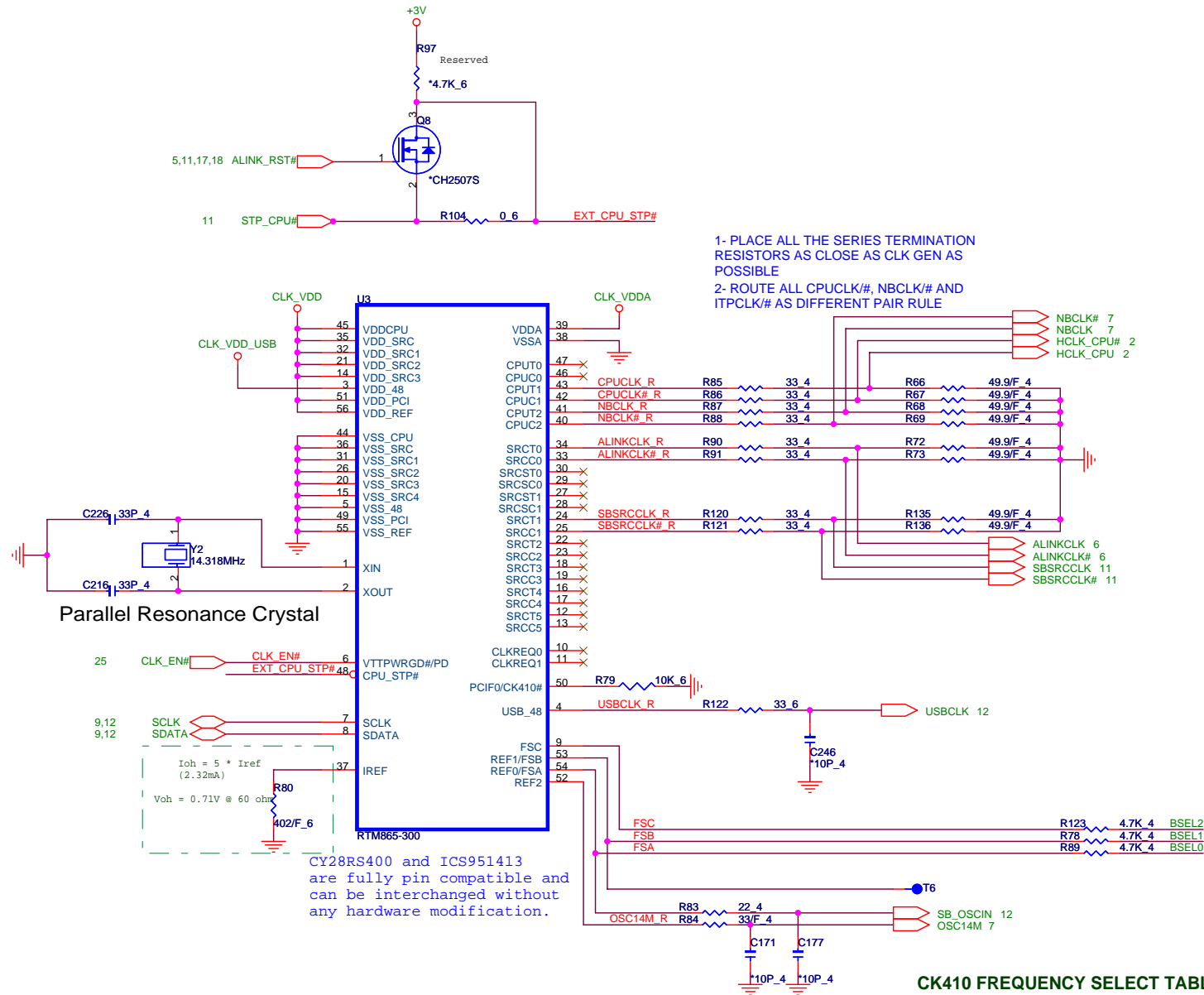


22uF 0805 X6S->105 degree C  
8 inside cavity north side secondary layer, 8 inside cavity south side secondary layer, 6 inside cavity north side primary layer, 6 inside cavity south side primary layer.



CPU

# CLK

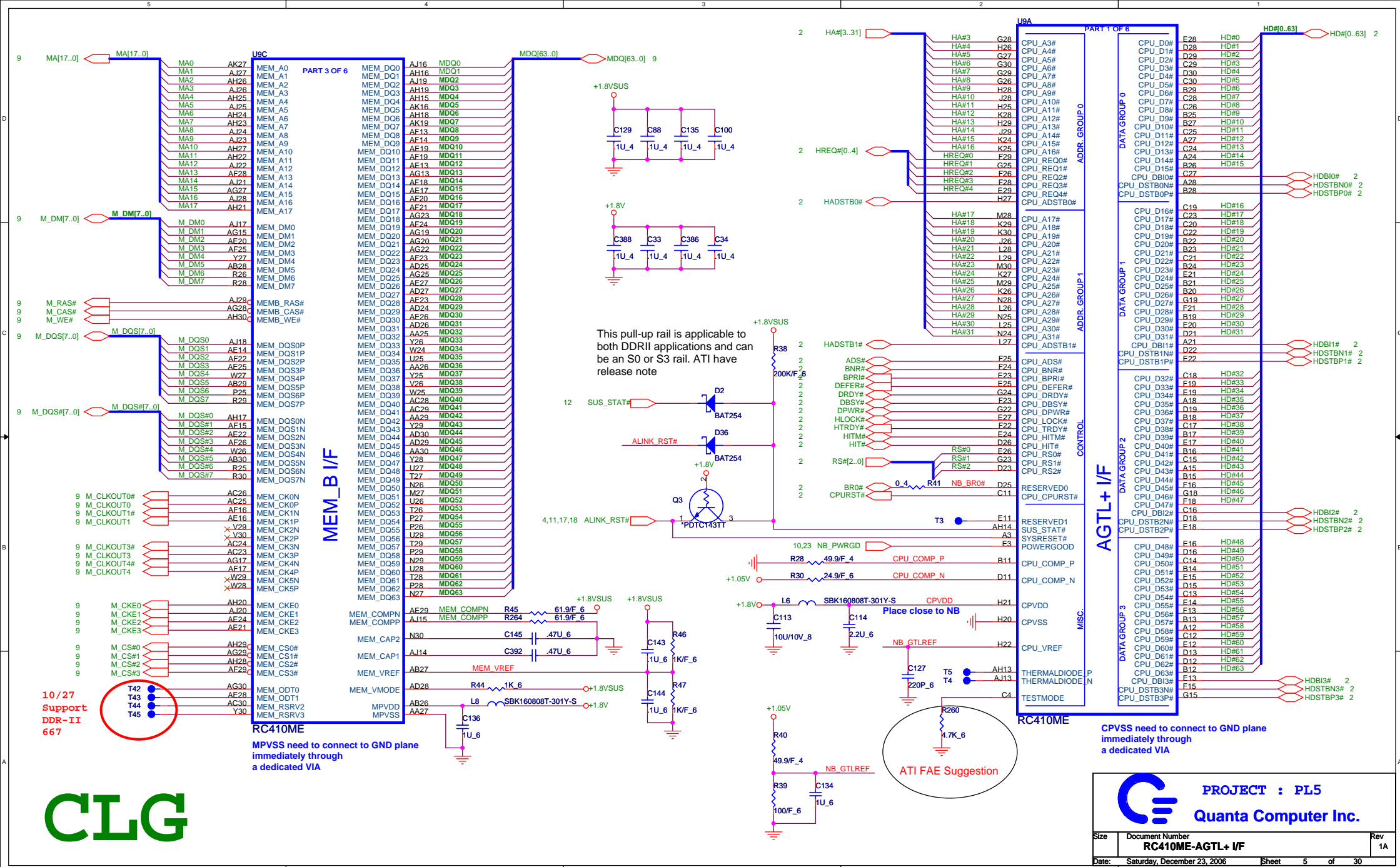


CK410 FREQUENCY SELECT TABLE(MHZ)

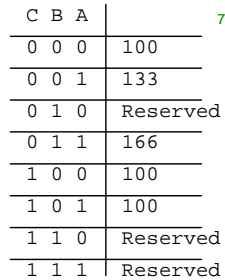
FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31



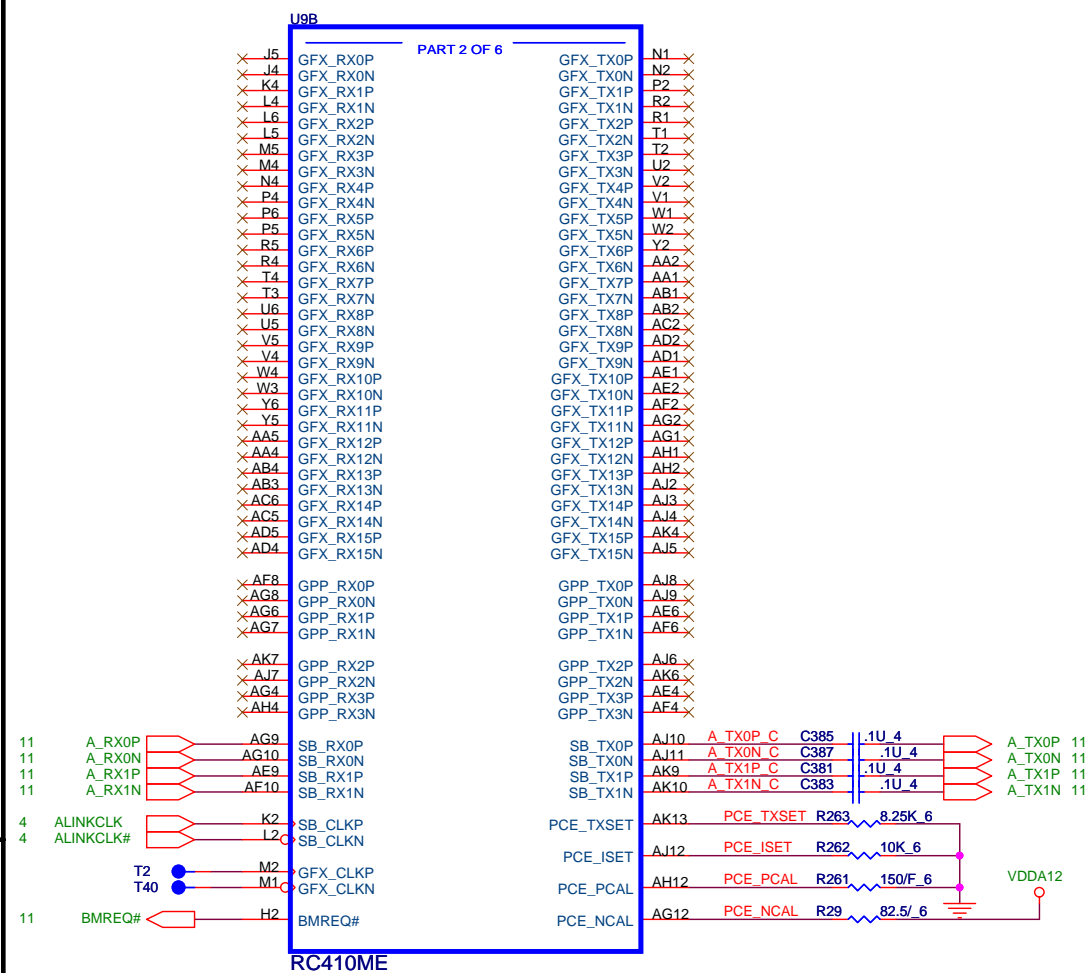
PROJECT : PL5  
Quanta Computer Inc.



# CLG

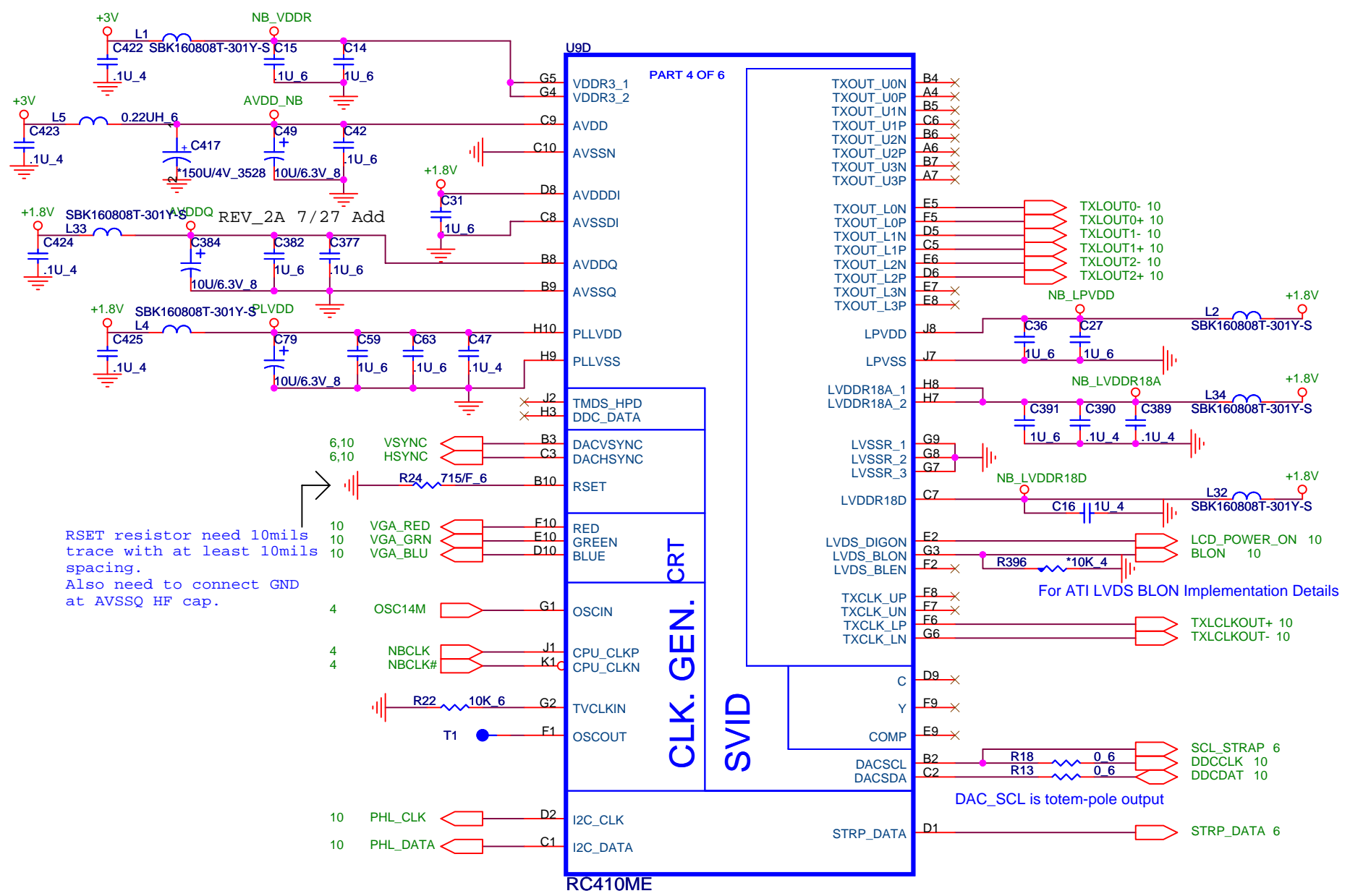



```
STRP_DATA:Debug strap
DEFAULT:1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING
```





CLG





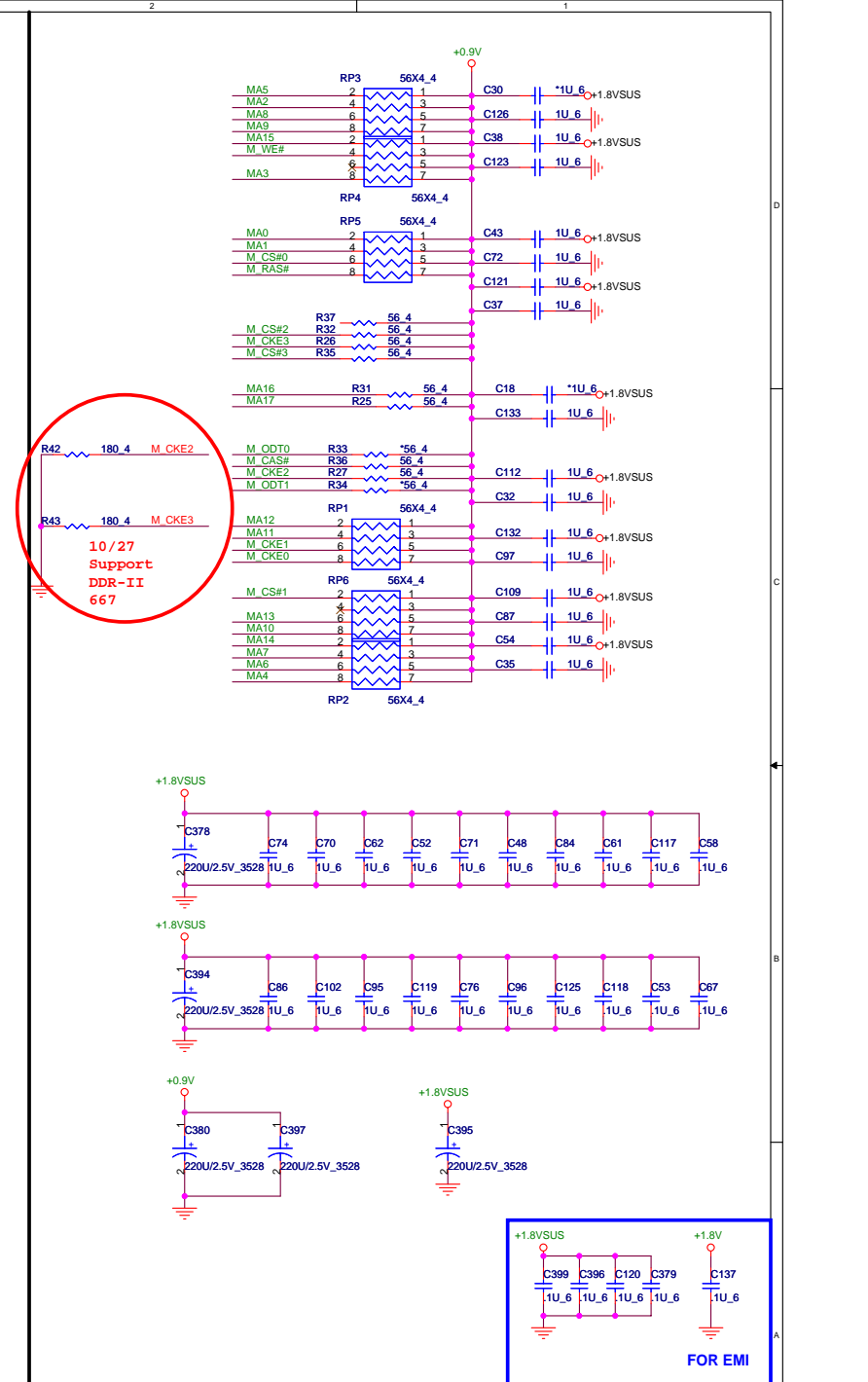
PROJECT : PL5

Quanta Computer Inc.

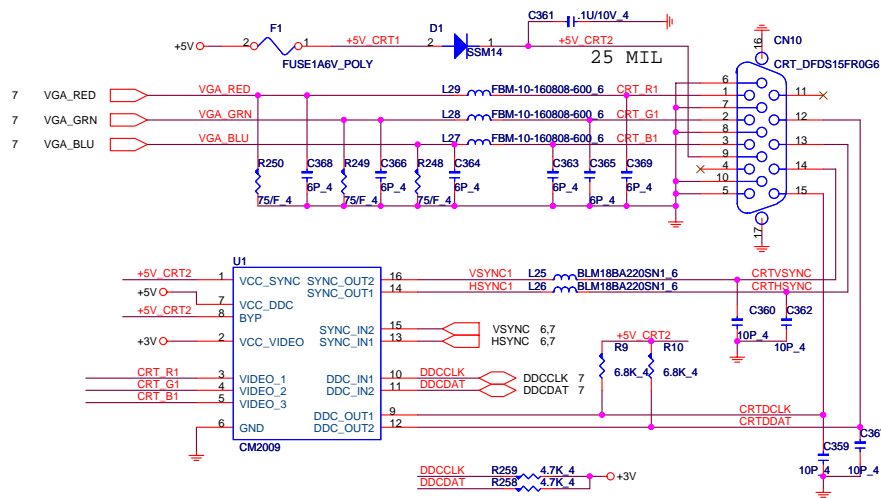
Size	Document Number	Rev
	<b>RC410MD-VIDEO &amp; CLKGEN</b>	1A
Date:	Saturday, December 23, 2006	Sheet 7 of 30



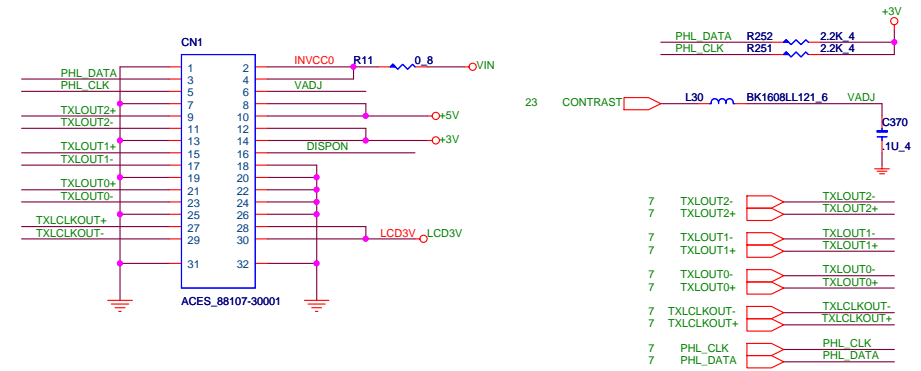




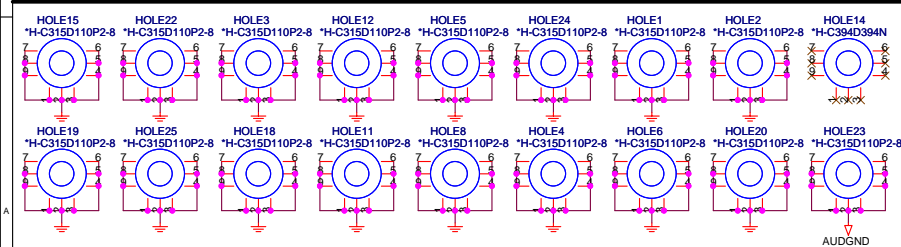
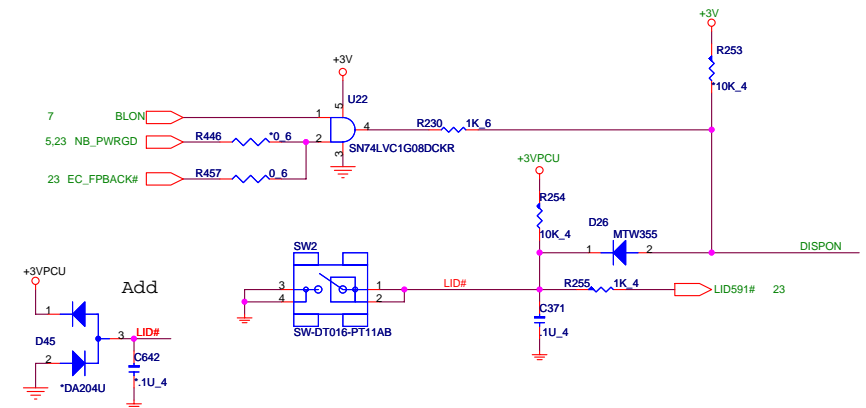
## CRT PORT



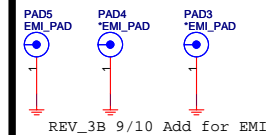
## LCD Connector



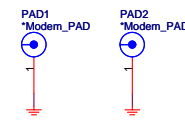
## Lid Switch



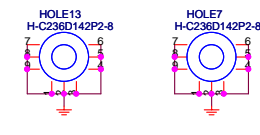
## EMI PAD



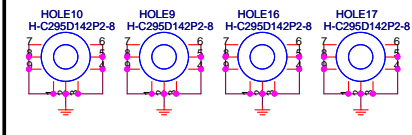
## Modem



## NB SINK



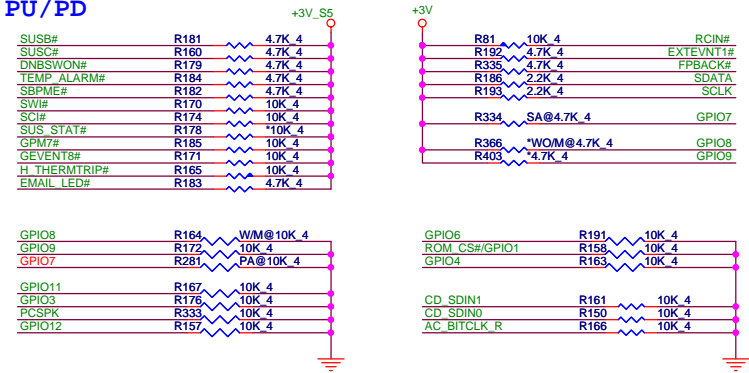
## CPU SINK



PROJECT : PL5  
Quanta Computer Inc.

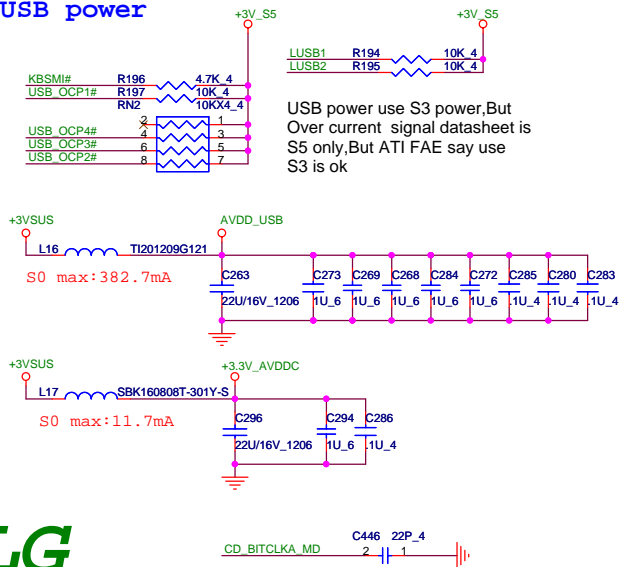
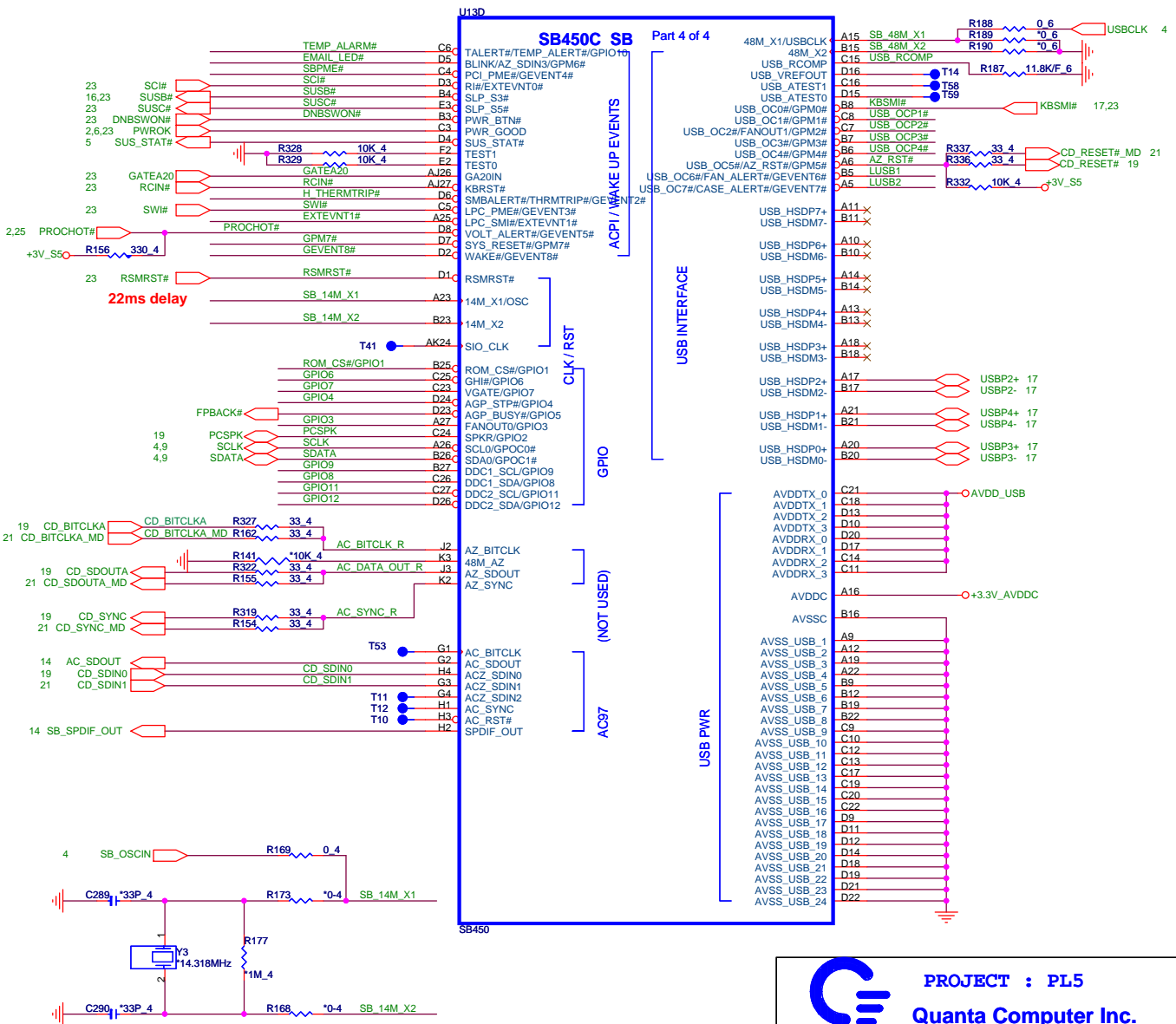


PU / PD



Configuration Table	GPIO9 PIN	GPIO8 PIN	GPIO7 PIN
<b>CRT (default)</b>	LOW		
W/O CRT	HIGH		
<b>Modem (default)</b>		LOW	
W/O Modem		HIGH	
<b>PATA HDD</b>			LOW
<b>SATA HDD</b>			HIGH

USB power

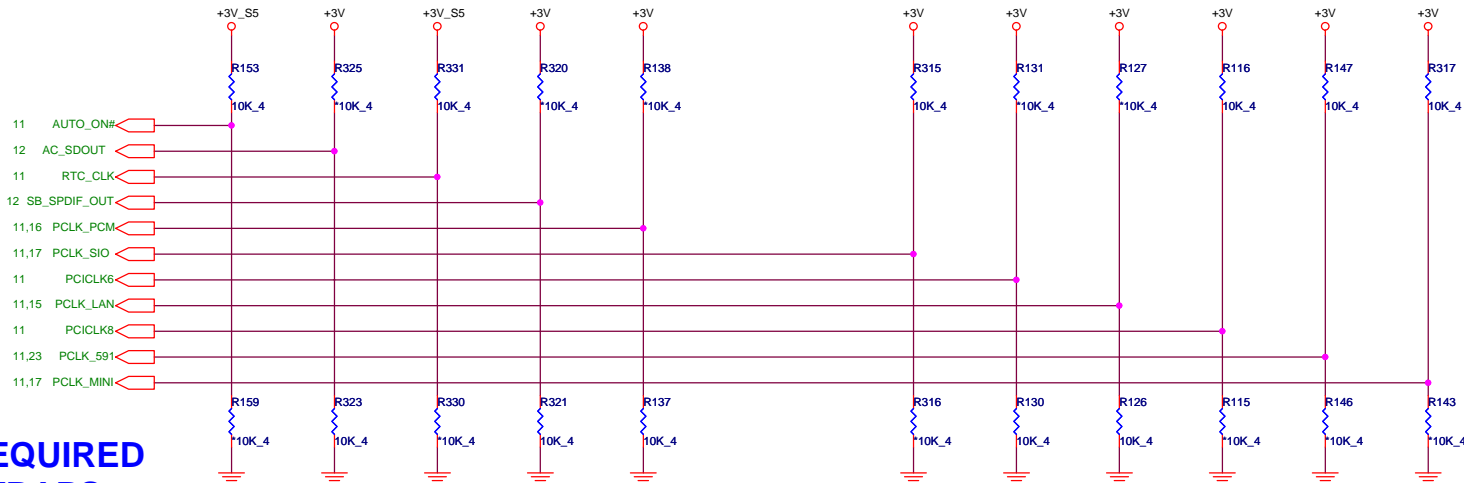
**CLG**

PROJECT : PL5  
Quanta Computer Inc.

Size Custom	Document Number <b>SB450C ACPI/GPIO/USB/AC97</b>	Rev 1A
Date:	Saturday, December 23, 2006	Sheet 12 of 30



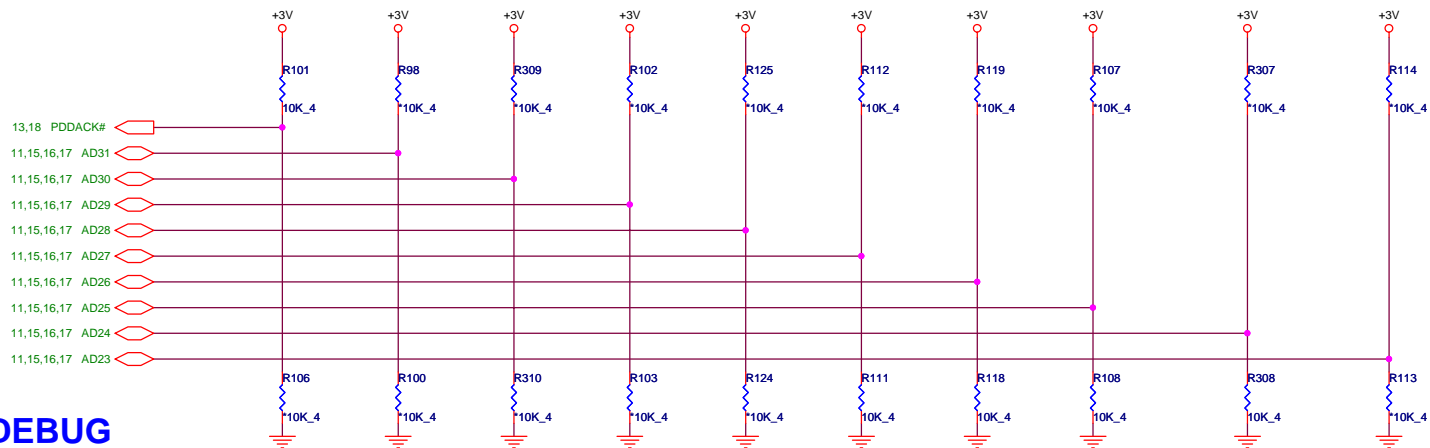
## REQUIRED STRAPS



					PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI*
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	H,H = PCI(X BUS) ROM H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE DEFAULT	48MHz Crystal Pad DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712 )	SIO 48MHz DEFAULT	48MHz use External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.

## DEBUG STRAPS

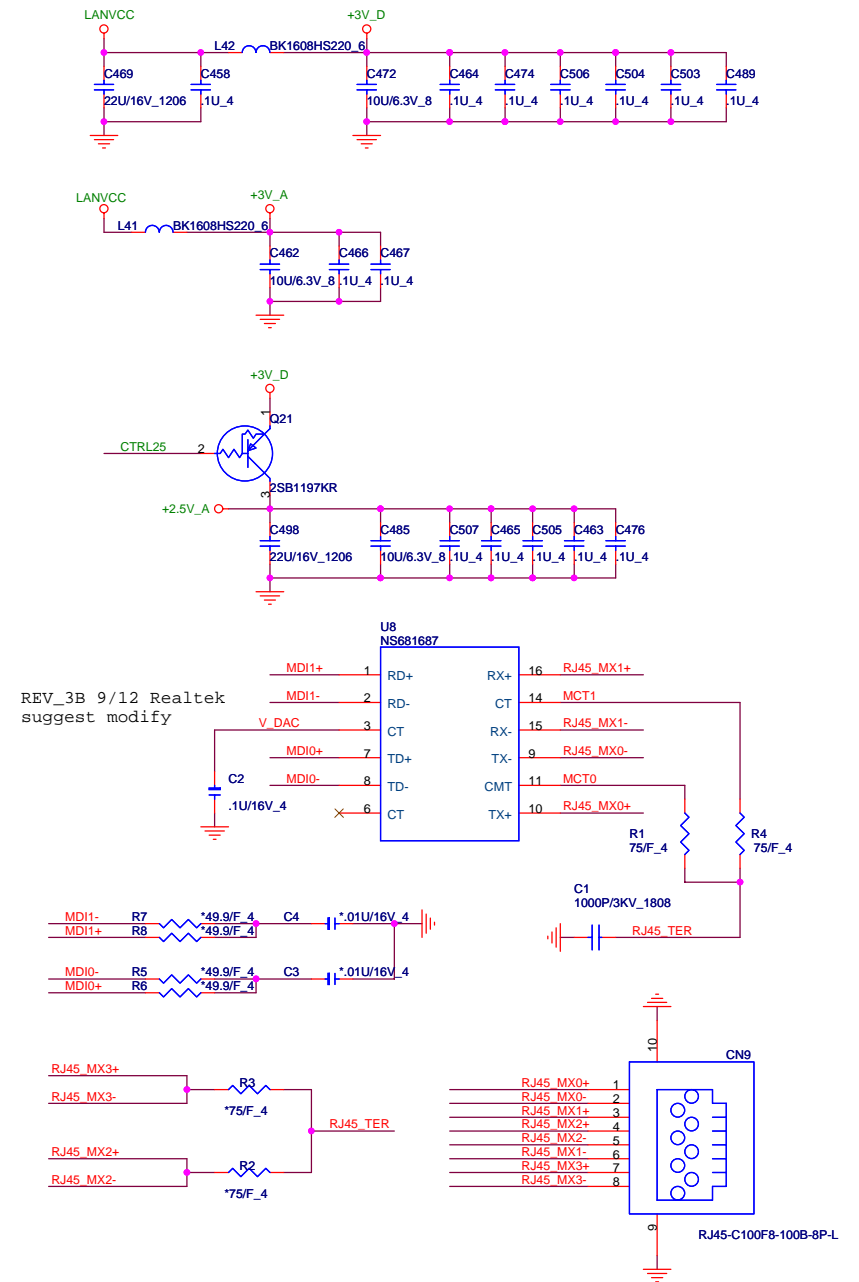
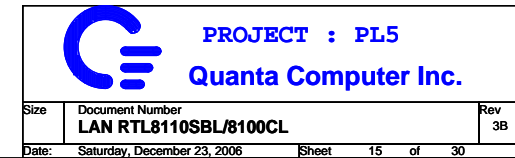


	PBACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

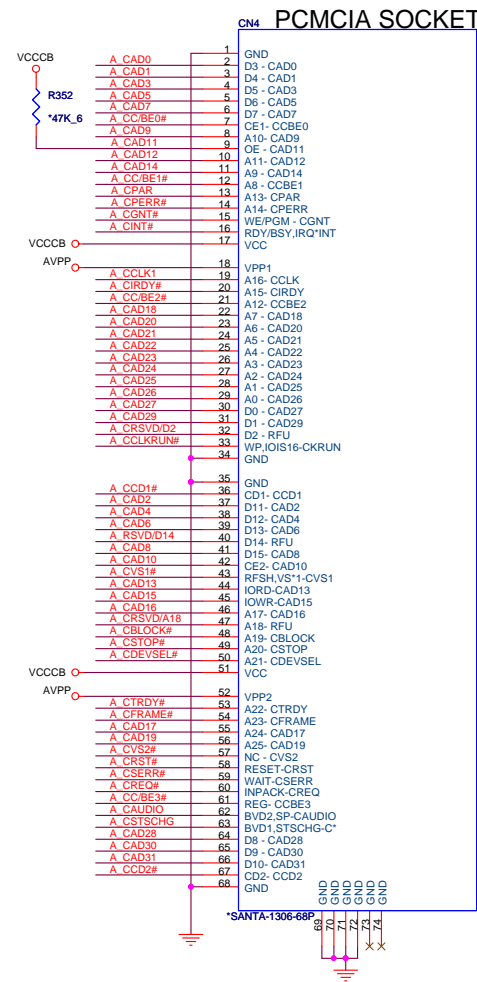
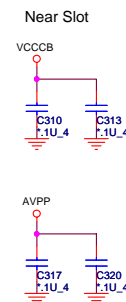
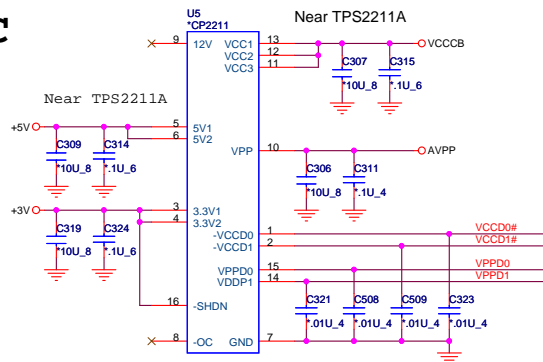
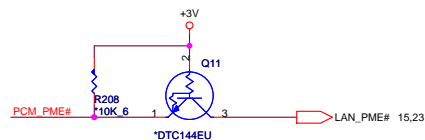
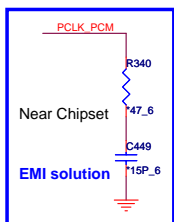
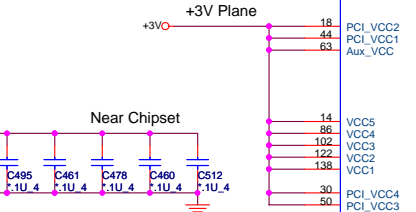
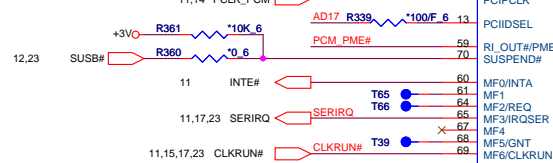
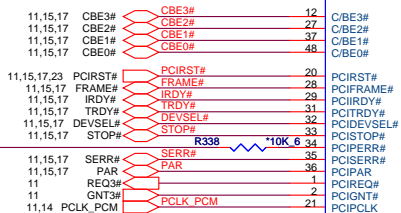
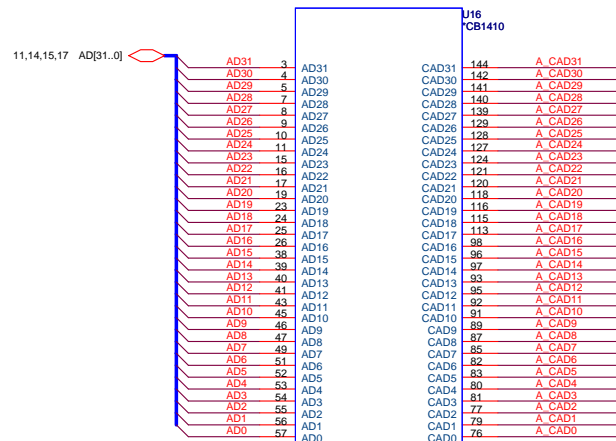
CLG



# LAN



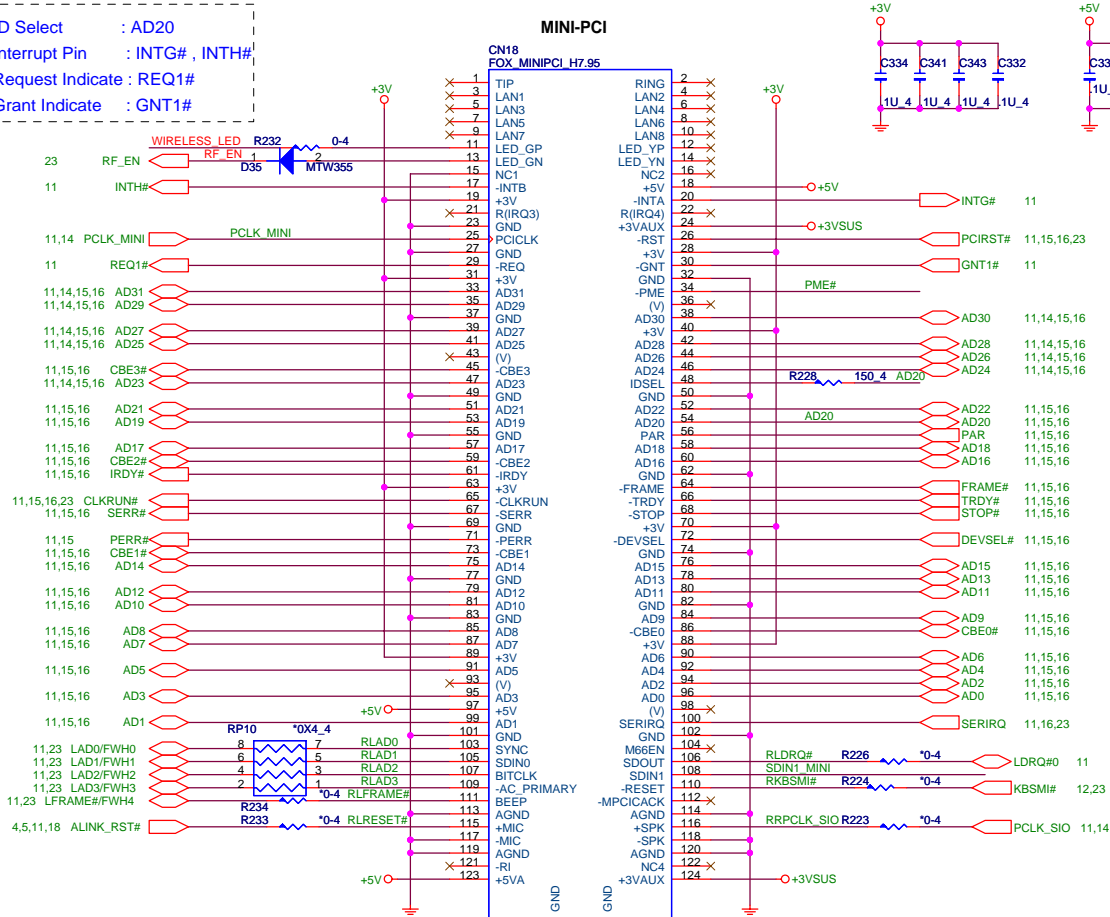
**This Page Function NC**



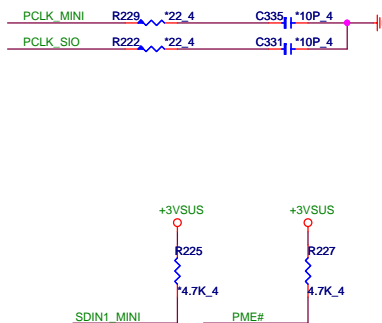
**CBS**

ID Select : AD20  
 Interrupt Pin : INTG# , INT#  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#

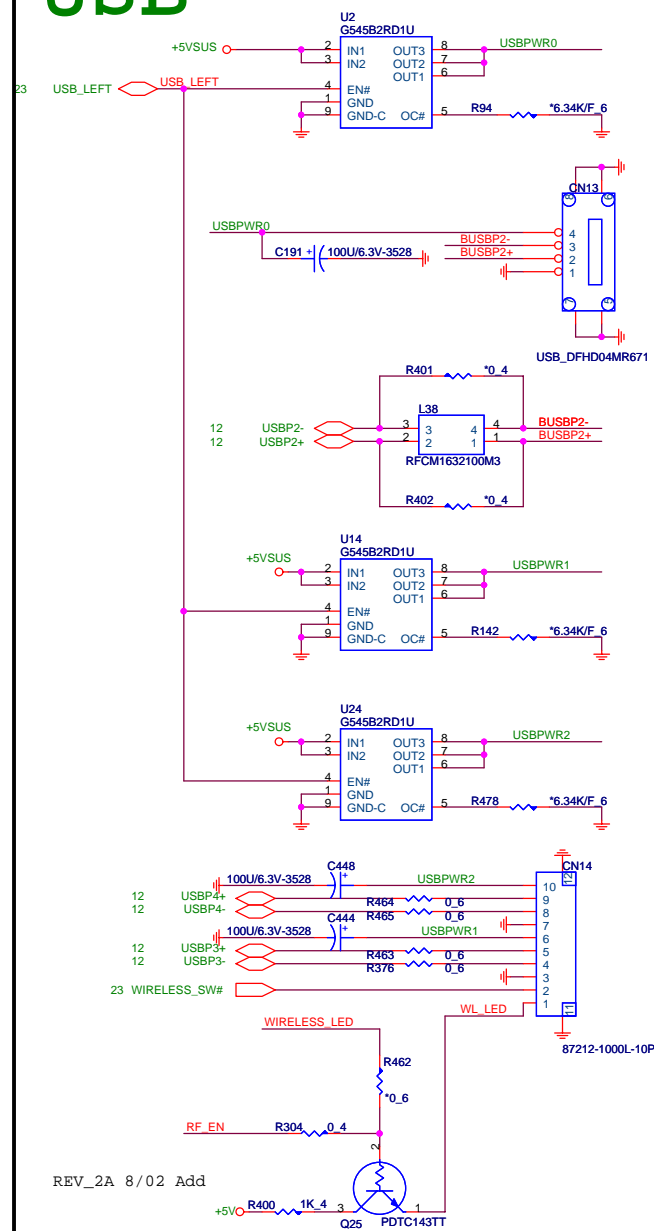
## MINI-PCI



## MPC

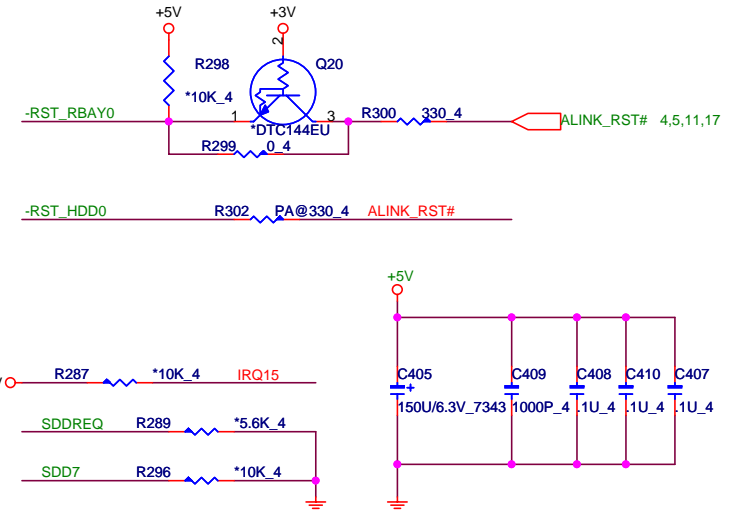
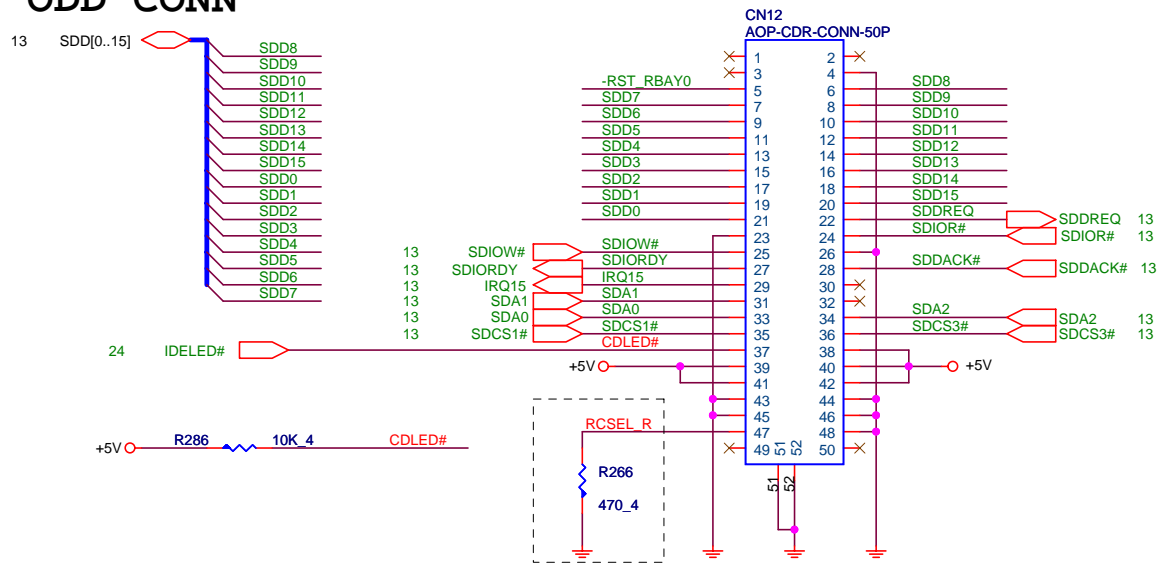


## USB

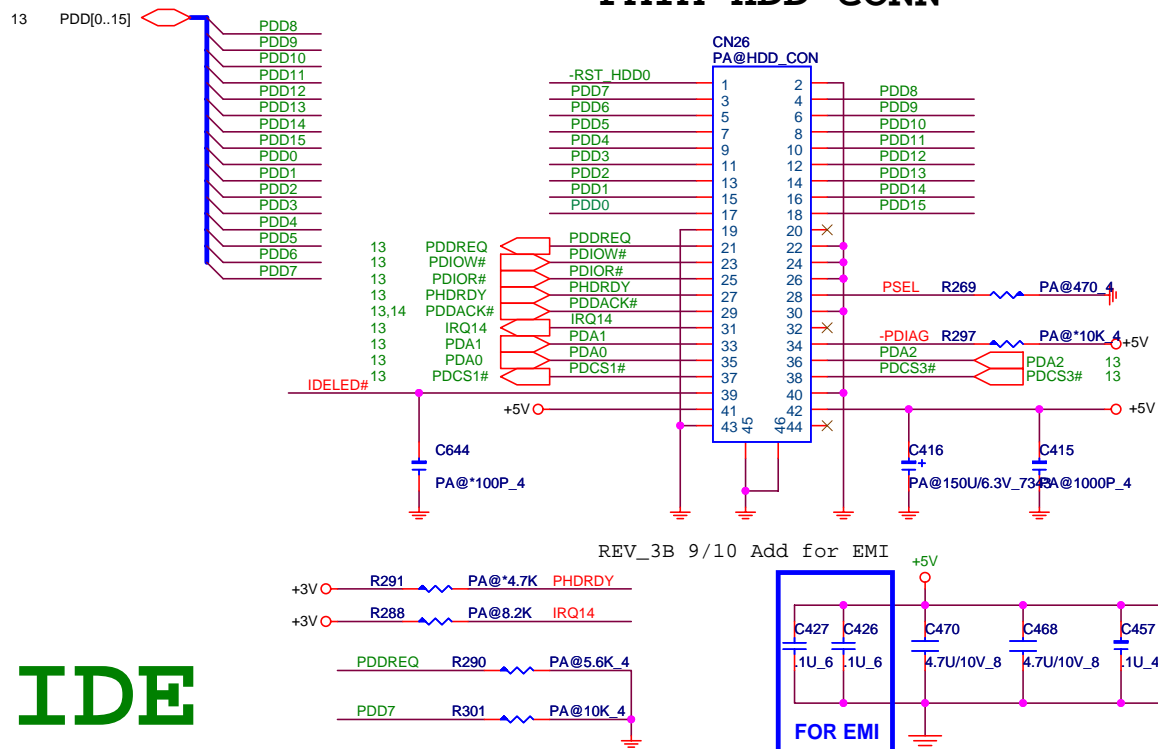


PROJECT : PL5  
 Quanta Computer Inc.

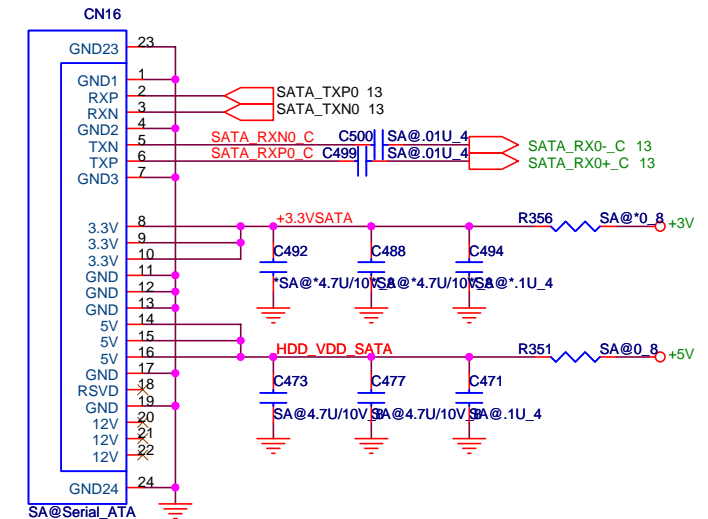
# ODD CONN



# PATA HDD CONN



# SATA HDD CONN



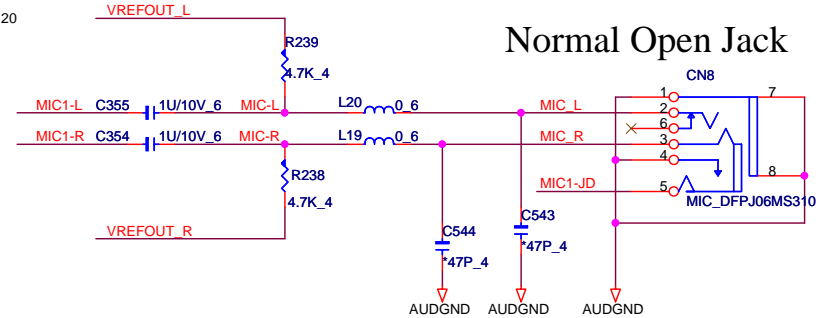
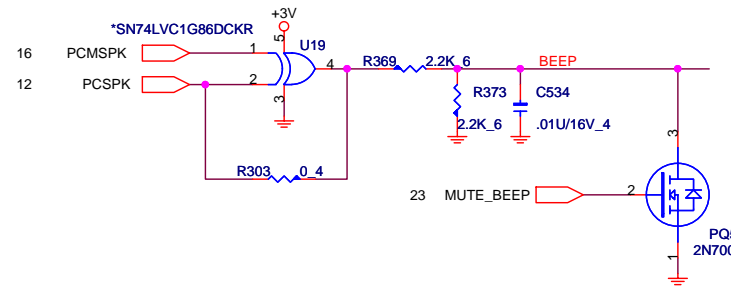
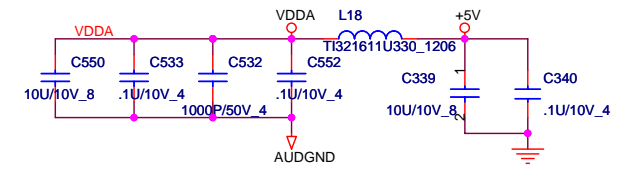
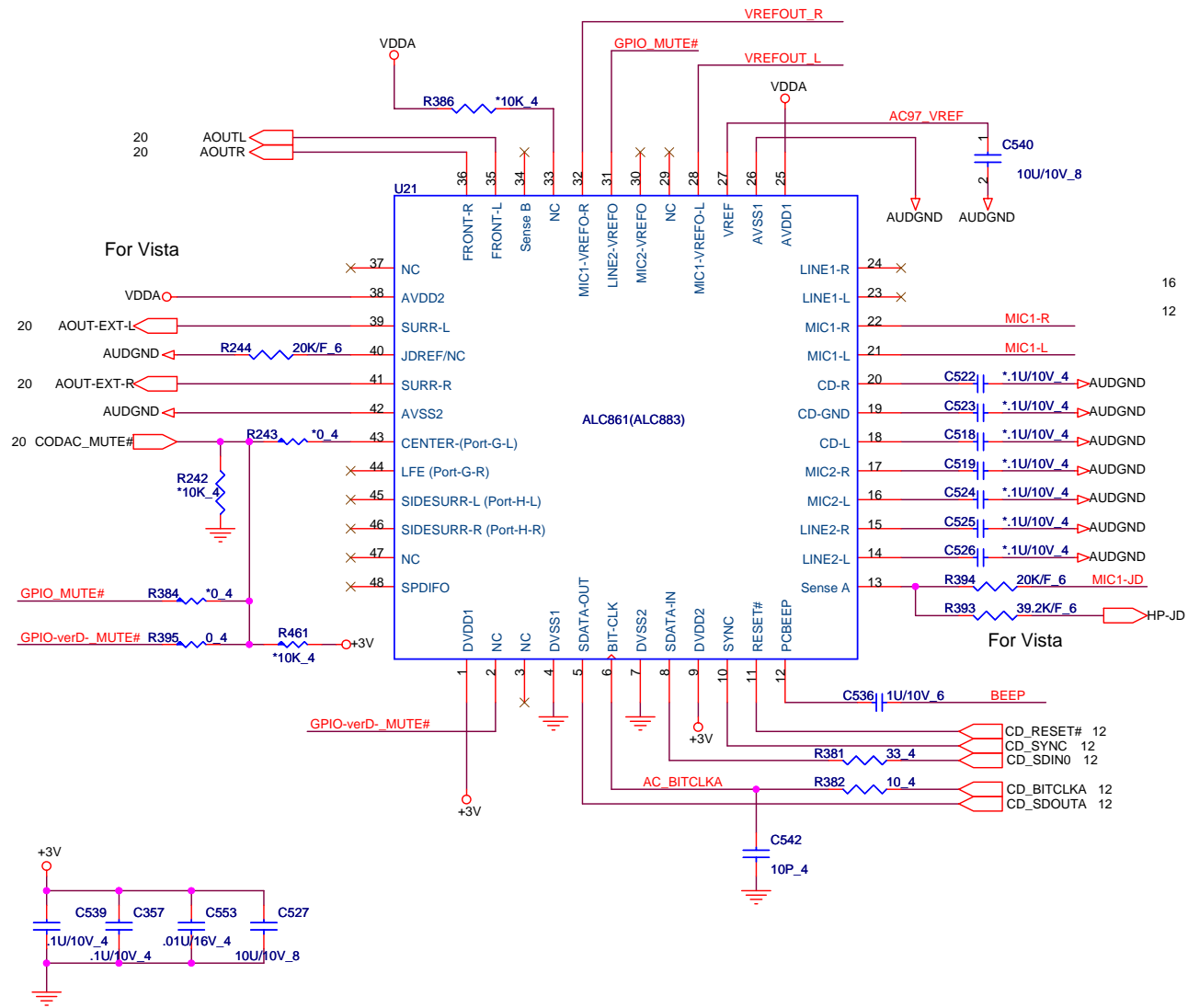
IDE




PROJECT : PL5  
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM	1A
Date:	Saturday, December 23, 2006	Sheet 18 of 30

ADO

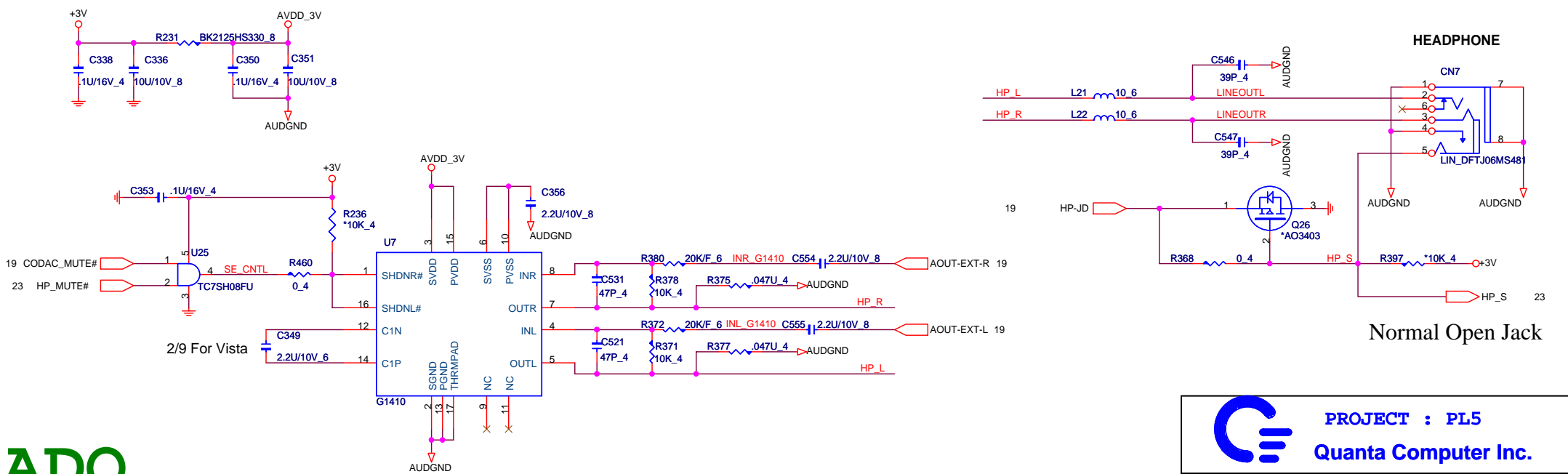
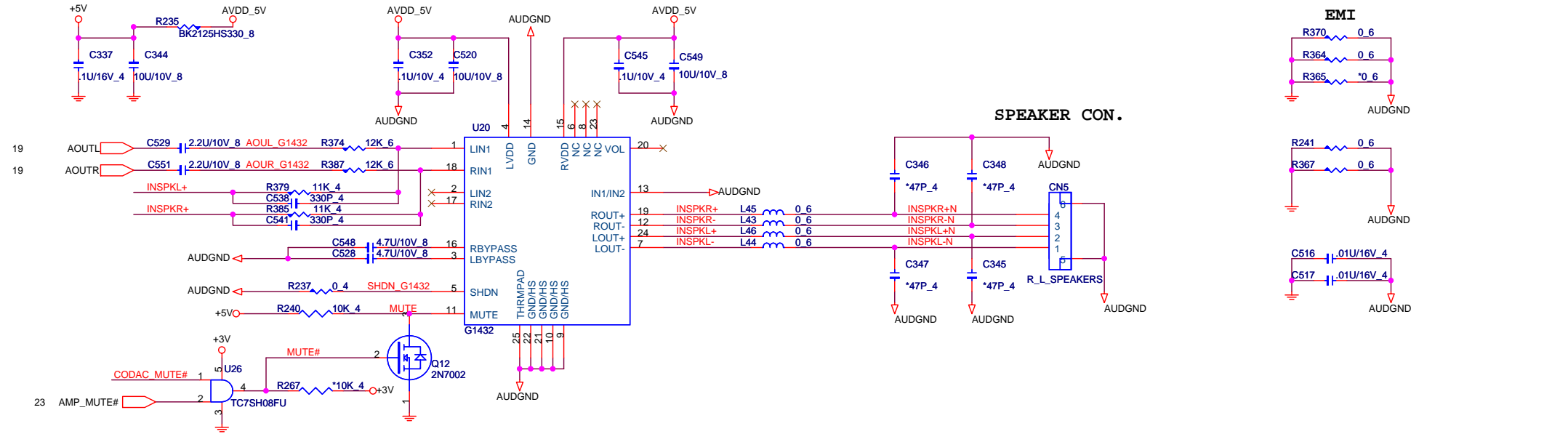




PROJECT : PL5

Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC861	1A
Date:	Saturday, December 23, 2006	Sheet 19 of 30



ADO

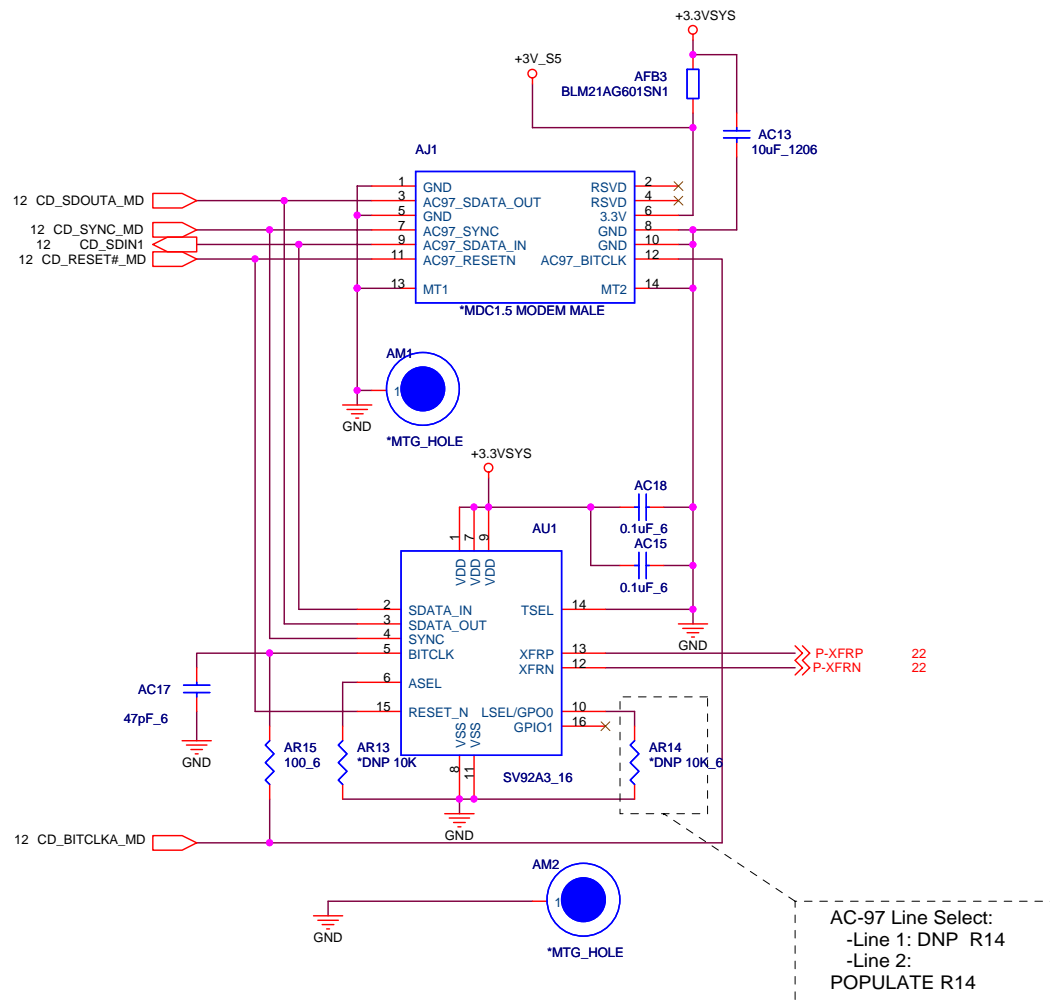
**PROJECT : PL5**

**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AUDIO AMP(G1432 / G1410)</b>	<b>1A</b>
Date:	Saturday, December 23, 2006	Sheet 20 of 30

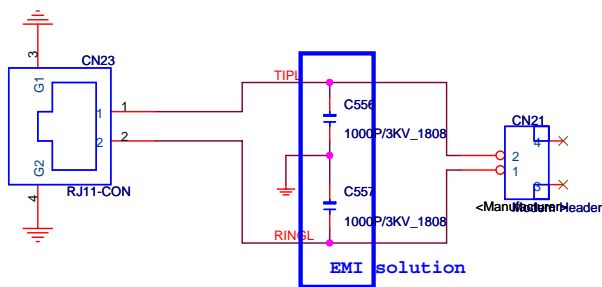


MDM

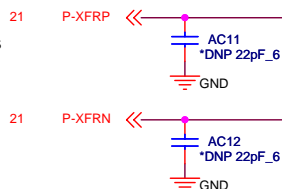


Agere Systems Holmdel NJ		agere systems	
Design Engineer: C. Russo		Title	
DELPHI SV92A3 MDC 1.5 Reference Design		Rev 1A	
Size B	Document Number	Date: Saturday, December 23, 2006	
DIGITAL INTERFACE		Sheet 21	of 30

Agere Systems Proprietary  
 DRAFT COPY - FOR REVIEW ONLY  
 SUBJECT TO CHANGE



Locate C11, C12 as close to digital device as possible.

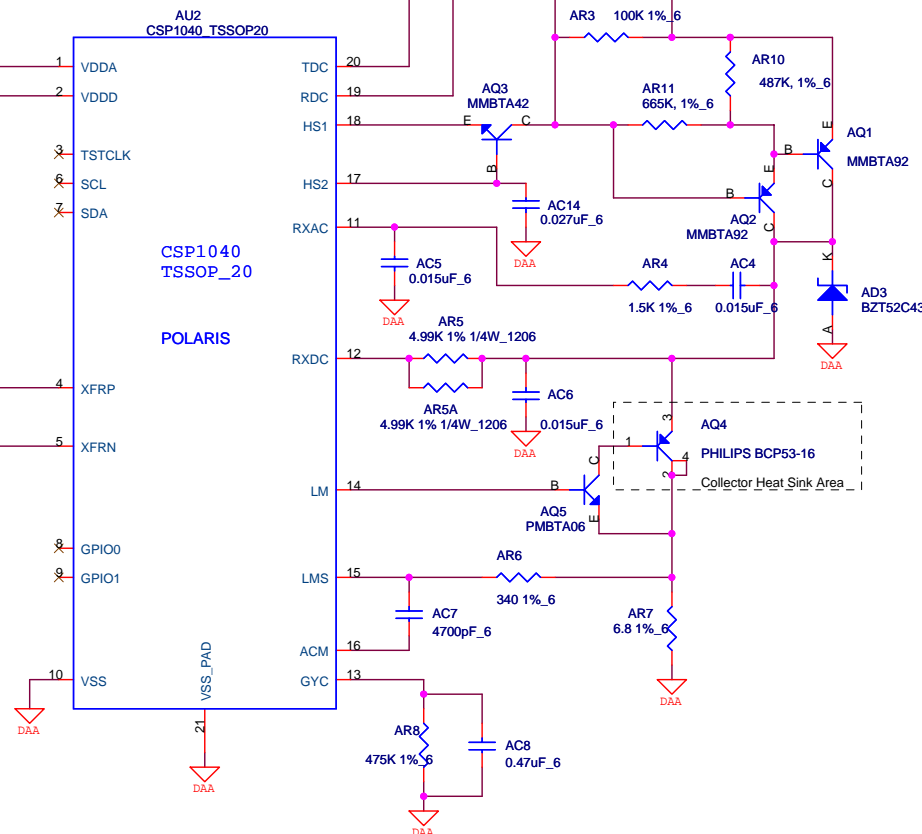


# MDM

## FUSE Note:

The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

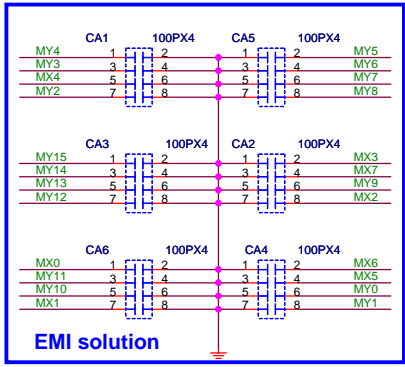
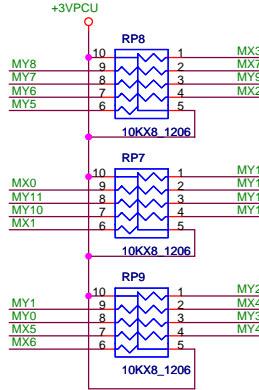
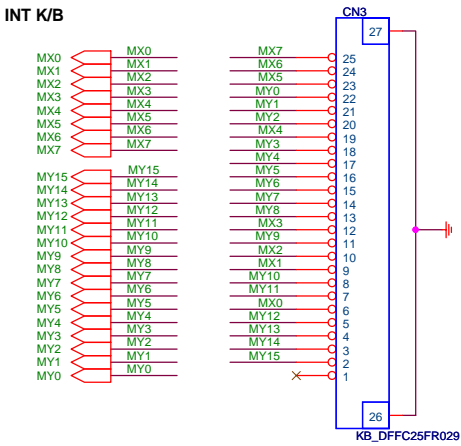
Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



<b>Agere Systems</b> Holmdel NJ		
<b>Design Engineer: R. Trevino</b>		
<b>DELPHI SV92A3 MDC 1.5 Reference Design</b>		
Size B	Document Number <b>CSP1040 DAA</b>	Rev 1A
Date:	Saturday, December 23, 2006	Sheet 22 of 30

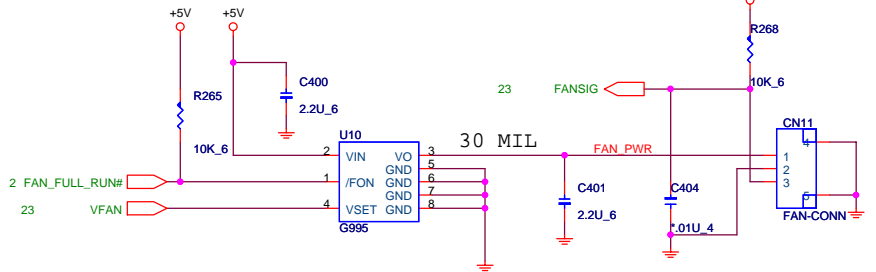
Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE





KBC

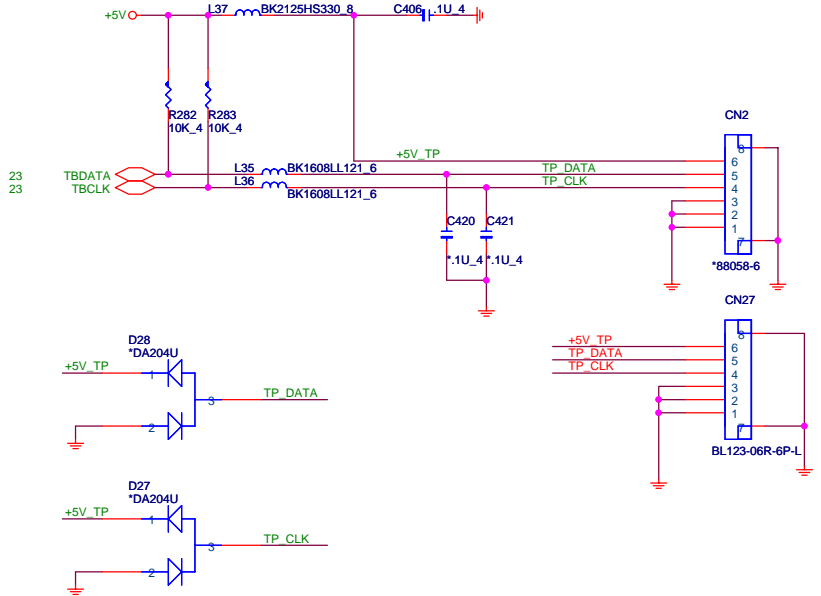
FAN CONTROL



THM

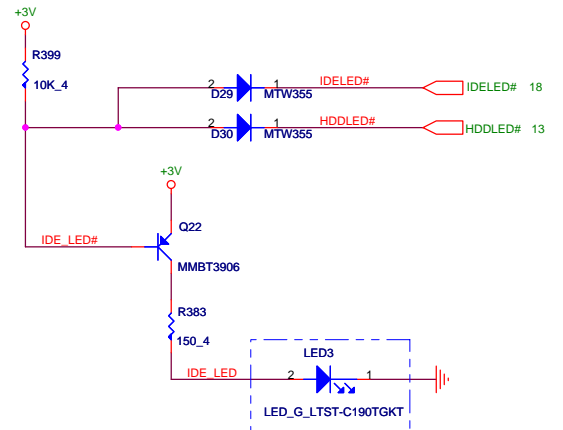
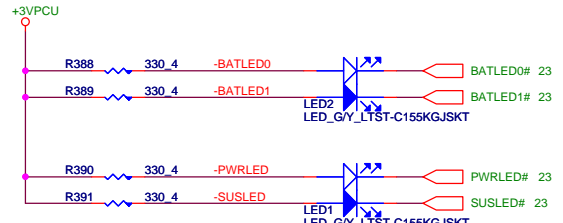
TOUCH PAD

20 MIL

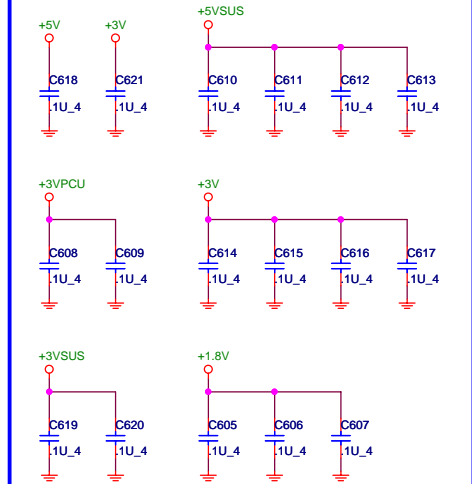


TPD

ON BOARD LED

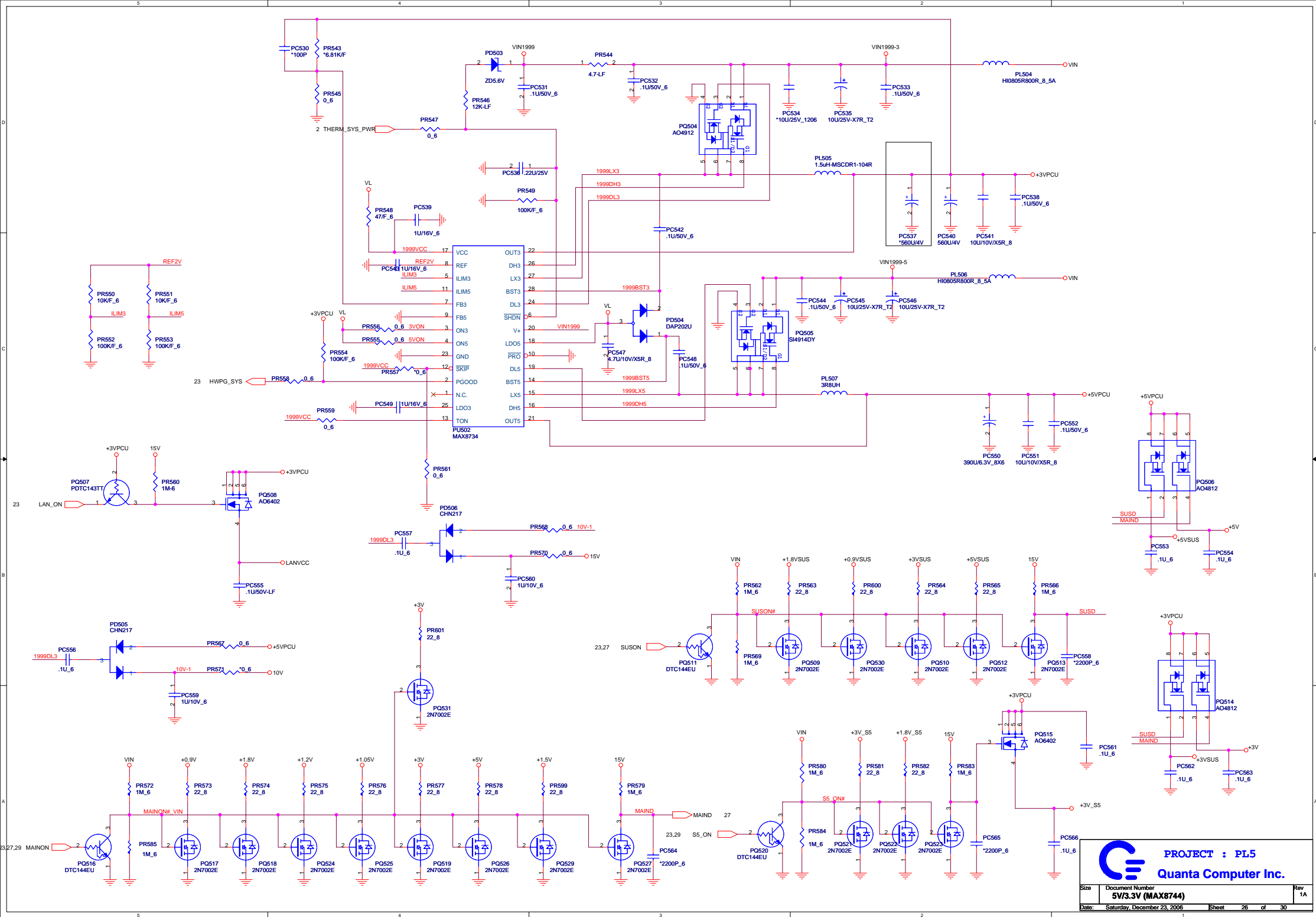


EMI solution



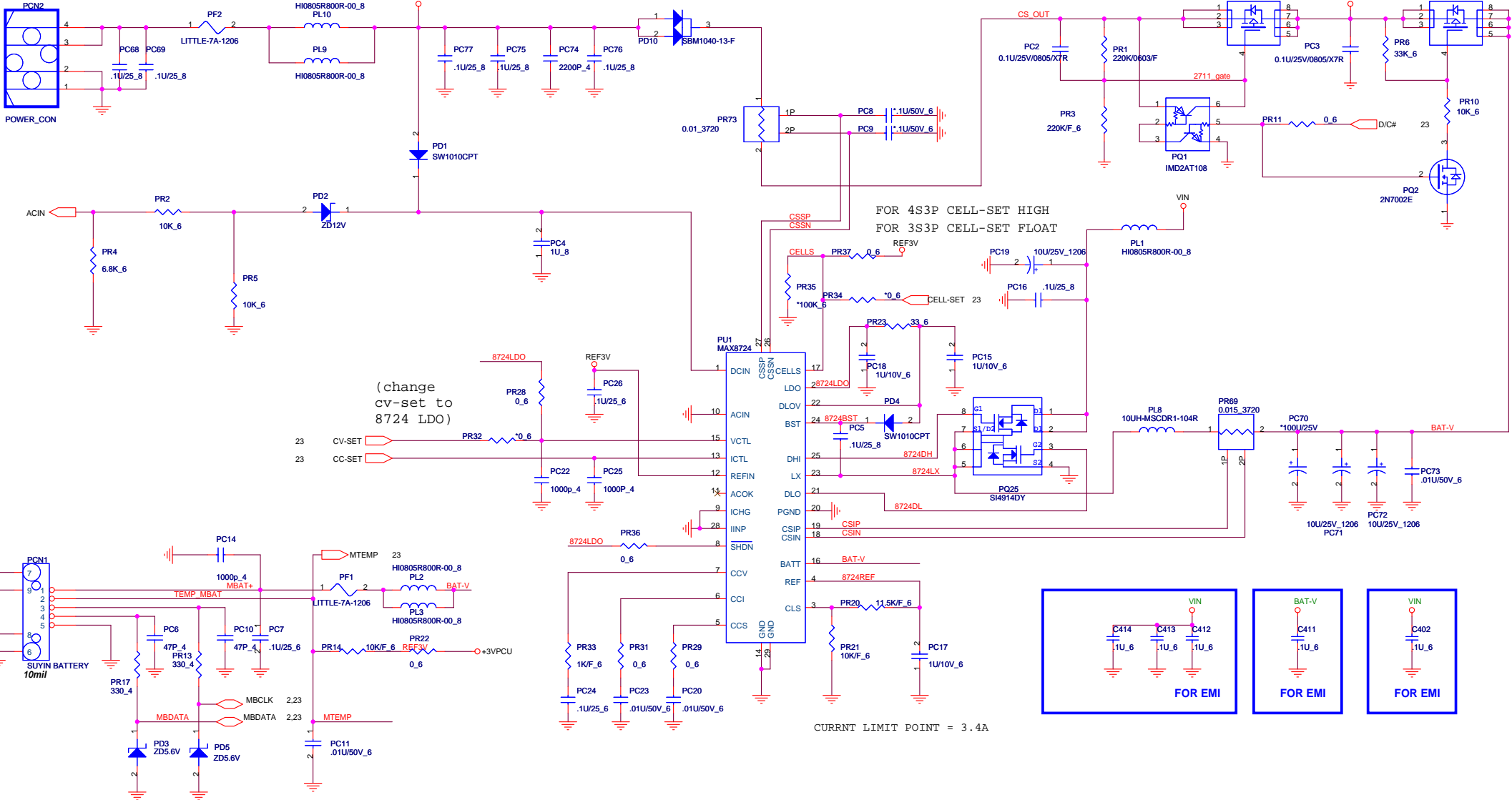
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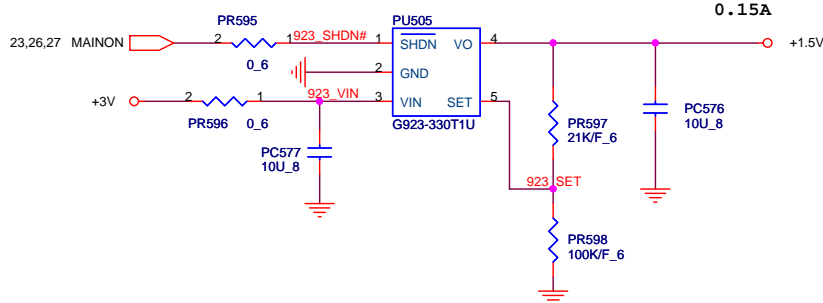
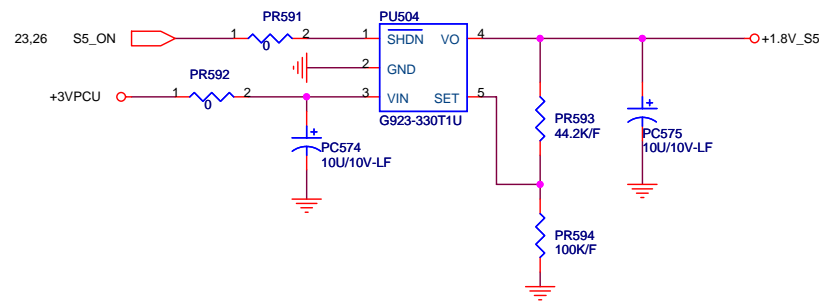
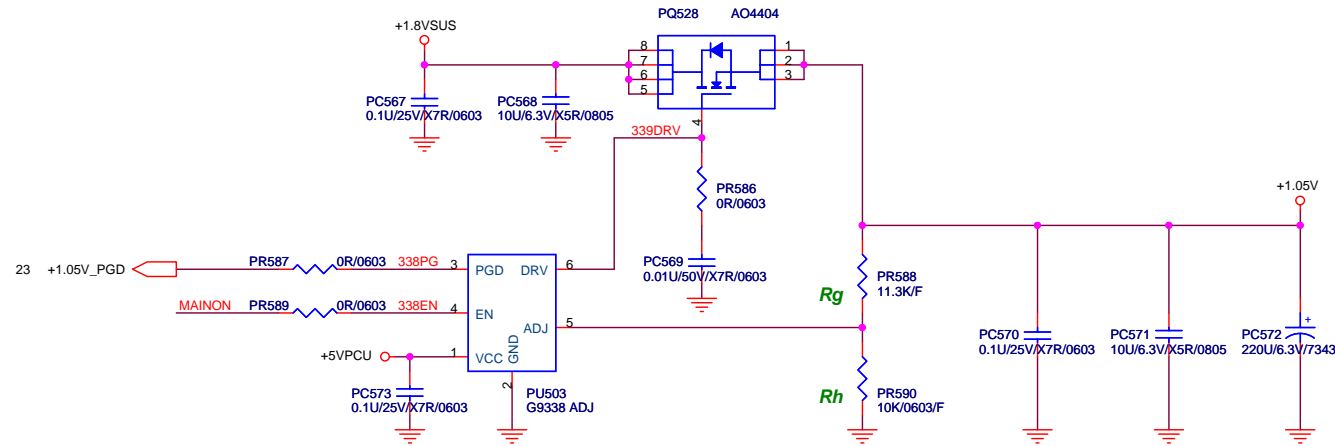


DCD



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